IN THE CLAIMS:

1. (Previously presented) A communication system for communicating digital information, the communication system comprising a digital adapter (5) and an analog adapter (6), wherein the digital adapter (5) is linked to a digital exchange (3) by means of a digital interface (7) and the analog adapter (6) is linked to an analog exchange (4) by means of an analog interface (8), said exchanges (3,4) being linked by means of a telecommunications network (2), wherein said digital adapter and analog adapter include link means (11,12;15,16) for linking between the digital adapter (5) and the analog adapter (6), the digital information from the digital adapter (5) being sent to the analog adapter (6), and vice versa, in a digital form without emulating an analog signal.

2. (Previously presented) A system according to claim 1, wherein said link means (11,12;15,16) include, in the direction of transmission going from the digital adapter (5) to the analog adapter (6), a digital transmitter (11) situated in the digital adapter (5) and able to transmit, to an analog receiver (15) situated in the analog adapter (6), analog pulses the voltage levels of which represent the digital information transmitted from the digital adapter (5) to the analog adapter (6).

3. (Previously presented) A system according to claim 1, wherein said link means (11,12;15,16) include, in the direction of transmission going from the analog adapter(6) to the digital adapter (5), an analog transmitter (16) situated in the analog adapter (6) and able to transmit, to a digital receiver (12) situated in the digital adapter (5), an analog signal such that, when the analog signal is sampled by the analog interface of the exchange (4), the sample of the analog signal will equate to the sum of a value able to be determined by the digital information transmitted by the analog adapter (6) to the digital adapter (5) and of the echo of the signal transmitted by the digital adapter (5), without said value having to be equal to a level of a quantization law.

4. (Previously presented) A system according to claim 1 or claim 2, wherein the receiver of the analog adapter (6) includes an adaptive linear equalizer (17) connected at its input to the output of an analog/digital converter (19), and connected at its output to the input of an output equalizer (20) linked to the user's equipment, so

that the response at the output of the adaptive linear equalizer (17) is a partial response, in particular a class IV response.

5. (Previously presented) A system according to claim 4, wherein said partial response is determined adaptively.

6. (Previously presented) A system according to claim 4 or claim 5, wherein said output equalizer (20) is a decision feedback equalizer or a Viterbi equalizer.

7. (Previously presented) A system according to claim 1 or claim 2, wherein said means (11, 12) include, at the digital adapter (5) end, an n-level selector (14), n being equal, particularly, to 64, said levels being represented in the form of a byte, from among N = 256 possible quantization levels, said level selector (14) being connected, at its input, to the user's equipment and, at its output, to a digital interface.

8. (Previously presented) A system according to claim 3, wherein said transmitter (16) of the analog adapter (6) includes a line coder (27) followed by a predistortion filter (24) which synthesizes a partial response, in particular a class IV response.

9. (Previously presented) A system according to claim 8, wherein said partial response is determined adaptively.

10. (Previously presented) A system according to claim 1 or claim 3 wherein the digital adapter (5) includes a decoder (30) connected, at its input, to an echo filter (22) and to the output of the digital interface of the digital adapter (5), said decoder (30) delivering at its output to the user's equipment (9) the most likely sequence of groups of bits transmitted by the analog adapter (6), given the echo of the signal produced by the digital adapter (5).

Claim 11 is cancelled.

12. (Currently amended) A method of transmission from an analog adapter (6) to a digital adapter (5) in a communications system, said method including in the analog adapter the steps of:

- taking a succession of groups of bits from digital information originating from a data source connected to the analog adapter; and

- generating ~~a a succession~~ a succession of analog signals synchronized to a clock of the digital adapter, wherein each analog signal has an amplitude corresponding to a digital value of one of the groups of bits, wherein the successive analog signals interfere with one another, forming a resulting analog signal at an analog interface of an analog exchange of the communication system, and have a shape such that, at the moment when said resulting analog signal is sampled in the analog interface of the exchange, said resulting analog signal is substantially equal to the sum of a value determined by the digital information and of the echo of a signal being transmitted by the digital adapter (5), without said value having to be equal to a level of the quantization law, so that following the sampling of the resulting analog signal, a byte appears in the digital adapter (5), representing said sum.

13. (Currently Amended) An analog adapter (6) for use in a communication system, wherein ~~the~~ a digital adapter (5) of the communication system may be linked to a digital exchange (3) by means of a digital interface (7), and the analog adapter (6) may be linked to an analog exchange (4) by means of an analog interface (8), said exchanges (3,4) being linked by means of a telecommunications network (2), wherein said analog adapter includes at least a means (15) for receiving digital information from the digital adapter (5) being sent to the analog adapter (6) at a rate of at least 8000 digital information bearing symbols per second, wherein said means (15) forms a portion of the analog adapter (6) and includes an adaptive linear equalizer that forms a partial response output.

14. (Previously presented) The device according to claim 13, wherein the information in each information bearing symbol is a group of bits originating from a digital data source and each information bearing symbol is a voltage level determined by choosing one voltage level from among a plurality of voltage levels that corresponds to the group of bits, a sequence of the voltage levels each said voltage level represented in digital form by one byte and being transmitted 8000 times per second.

15. (Currently Amended) The method according to claim 12, further comprising in the digital adapter the steps of:

- processing the successive ~~bytes~~ groups of bits so as to retrieve the most likely sequence of the groups of bits, given the echo of the signal being transmitted by the digital adapter;

- transmitting the digital value of the groups of bits processed to an equipment of a user.

16. (Currently Amended) An analog adapter apparatus, comprising:

- means for taking a succession of groups of bits from digital information originating from a data source connected to the analog adapter system, each group of bits representing an item of the digital information to be transmitted to the digital adapter; and

- means for generating a succession of analog signals synchronized to a clock of the digital adapter, wherein each analog signal has an amplitude corresponding to a digital value of one of the groups of bits, wherein the successive analog signals interfere with one another, forming a resulting analog signal at an analog interface of an analog exchange of ~~the~~ a communication system, and have a shape such that, at the moment when said resulting analog signal is sampled in the analog interface of the exchange, said resulting analog signal is substantially equal to the sum of a value determined by the digital information and of the echo of a signal being transmitted by the digital adapter (5), without said value having to be equal to a level of the quantization law, so that following the sampling of the resulting analog signal, a byte appears in the digital adapter (5), representing said sum.